REMARKS

This responds to the Final Office Action dated September 1, 2006 (hereinafter "the Office Action"). Claims 25, 26, 29, and 30 are amended. Support for the amendments is found generally within the specification (see e.g., page 6 lines 1-20). Applicant respectfully requests the amendments to be entered by the Examiner for purposes of appeal. Claims 1-31 are pending in this application.

§102 Rejection of the Claims

Claims 1-3 and 14 were rejected under 35 USC § 102(b) as being anticipated by Fiedler (U.S. 5,726,588). Applicant respectfully traverses the rejection. The Office Action fails to establish a *prima facie* case of anticipation because Fiedler does not teach all of the elements recited in the claims.

Regarding claims 1-3:

Applicant cannot find in Fiedler any teaching of, among other things, an apparatus comprising,

> a first differential output driver to provide a single ended output voltage in response to an input voltage; and a second differential output driver to provide a single ended output in response to the input voltage,

as recited in claims 1-3. Fiedler says that a differential-to-CMOS level converter 10 is a balanced comparator with differential inputs 12a and 12b and complementary outputs 14a and 14b,[1] and that "converter circuit 32 is substantially the same as differential-to-CMOS level converter 10 shown in FIG. 1."[2] Thus, Fiedler only refers to one differential circuit. It is a converter circuit having complementary outputs and is not a "differential output driver to provide a single ended output voltage" as recited in claim 1.

In the Office Action, the "Examiner asserts that two complementary outputs, 14a and 14b, cannot be generated using a single differential circuit."[3] This assertion is presumably made to show that there must be two circuits in Fiedler, each providing one output. However, Fiedler states

[1] Fiedler, col. 2 lines 64-66.
[2] Fiedler, col. 3 lines 48-50.
[3] Office Action, pg. 2.

that "converter circuit 32 is substantially the same as differential-to-CMOS level converter 10 shown in FIG. 1"[4] and that "FIG. 1 is a schematic diagram of common differential-to-CMOS level converter 10 ... with ... complementary outputs 14a and 14b."[5] Therefore, Fiedler refers to a single converter circuit 32 that generates two complementary outputs. Fiedler states that "other [converter] circuit configurations can be used,"[6] but Fiedler contains no disclosure of other configurations.

Additionally, Applicant cannot find any disclosure of,

a feedback circuit to monitor the first and second output voltages and apply a bias voltage to at least one of the first and second output drivers,

as recited in claim 1. To anticipate a claim "the identical invention must be shown in as complete detail as is contained in the ... claim."[7] Fiedler refers to where a cross-over voltage adjustment circuit 36 monitors the cross-over voltage of the signals on circuit nodes N8 and $\overline{N8}$, compares the cross-over voltage to a reference voltage, and sources or sinks equal offset currents into or from circuit nodes N6 and $\overline{N6}$, in response to the comparison.[8] Thus, Fiedler does not teach the feedback structure recited in claim 1.

The Office Action states that in Fiedler "cross-over voltage adjustment circuit (36) is a feedback circuit having inputs N8 and complement of N8 derived from the outputs of 34b and 34d."[9] However, Fiedler does not show "a feedback circuit to ... apply a bias voltage to at least one of the first and second output drivers," as recited in claim 1.

Further, in regard to claim 3, Applicant can find no disclosure in the cited portions of Fiedler, of positive and negative conductors of a transmission cable, as recited in the claim 3. The Office Action states that this is described in Fiedler at col. 8 lines 12-15.[10] However, the cited portion only refers to "voltage supply terminals [that] can be relatively positive or relatively

[4] Fiedler, col. 3 lines 48-50.
[5] Fiedler, col. 2 lines 63-66.
[6] Fiedler, col. 3 lines 51-52.
[7] M.P.E.P. 2131 citing Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).
[8] Fiedler, col. 4 lines 11-15.
[9] Office Action, pg 2.
[10] Office Action, pg. 3.

negative, depending on the particular convention adopted and the technology used,"[11] and does not teach or suggest positive and negative conductors of a transmission cable.

Regarding claim 14:

Applicant cannot find in Fiedler any teaching or suggestion of, among other things, a method comprising,

> measuring a difference between a voltage at which output voltage signals of first and second drivers of a differential signal transceiver cross-over ... providing a correcting bias voltage proportional to a difference between the cross-over voltage and the equidistant voltage, and applying the correcting bias voltage to the differential drivers to vary the voltage point where the first and second output voltages cross-over,

as recited in claim 14. Instead, Fiedler compares the cross-over voltage to a reference voltage, and sources or sinks equal offset currents into or from circuit nodes N6 and $\overline{N6}$ in response to the comparison[12] instead of applying the correcting bias voltage to the differential drivers, as recited in claim 14.

Applicant respectfully requests reconsideration and allowance of claims 1-3 and 14.

§103 Rejection of the Claims

1. Claims 4-12 and 15-24 were rejected under 35 USC § 103(a) as being unpatentable over Fiedler as applied to claim 5 above.[13] Applicant respectfully traverses the rejection.

Claims 4-12 ultimately depend on base claim 1 and claims 15-24 ultimately depend on base claim 14. As set forth above, Applicant believes base claims 1 and 14 to be allowable at least for the reason that Fiedler does not teach or suggest all of the elements of those base claims.

Additionally, regarding claim 9, Applicant cannot find in Fiedler, among other things, any teaching or suggestion of an apparatus comprising,

> a differential receiver ... having a first output; a single-ended receiver ... having a second output; and a single-ended receiver ... having a third output; and wherein if the cross-over voltage is lower than the equidistant voltage, charge on the first capacitor is reduced while the first output is high and the second output is low

[11] Fiedler, col. 8 lines 16-18.
[12] Fiedler, col. 4 lines 11-15.
[13] Applicant assumes the Office Action intended to refer to Fiedler in regard to claims 1-3 and 14.

> and/or charge on the second capacitor is reduced while the first output is low and the third output is low,

as recited in claim 9. The Office Action asserts that single ended receivers for detecting rail-to-rail transitions are found in FIG. 2 of Fiedler.[14] However, Fiedler relates that FIG. 2 is a schematic diagram of a differential-to-CMOS level converter,[15] and that converter circuit 32 includes complementary output terminals 40a and 40b.[16] Thus, Fiedler does not teach or suggest a single ended receiver. Also, Applicant cannot find where "charge on the first capacitor is reduced while the first output is high and the second output is low and/or charge on the second capacitor is reduced while the first output is low and the third output is low," as recited in claim 9. Instead, Fiedler compares the cross-over voltage to a reference voltage, and sources or sinks equal offset currents into or from circuit nodes N6 and $\overline{N6}$ in response to the comparison.[17]

Further regarding claim 22, Applicant cannot find in Fiedler any teaching or suggestion of a method comprising,

> measuring a cross-over transition on positive and negative conductors ... measuring a rail-to-rail transition on the positive conductor ... and measuring a rail-to-rail transition on the negative conductor ... and wherein producing a net charge includes switching a charge onto the capacitor when there is a mismatch in transition times,

as recited in claim 22. Instead, Fiedler refers to a comparison of the cross-over voltage to a reference voltage,[18] rather than "a mismatch in transition times."

Applicant respectfully requests reconsideration and allowance of claims 4-12 and 15-24.

2. Claim 13 was rejected under 35 USC § 103(a) as being unpatentable over the combination of Haq and Fiedler as applied to claim 1 above, and further in view of Varma et al. (U.S. 6,946,904 B1, "Varma"). It is unclear from the Office Action whether the Examiner additionally relies on Komarek et al. (U.S. Pat. No. 6018219, "Komarek").[19] Clarification of whether the Examiner relies on Komarek, and what portion(s) of Komarek the Examiner believes is relevant to the

[14] Office Action, pg. 8.
[15] Fiedler, col. 3 lines 43-44.
[16] Fiedler, col. 3 lines 54-55.
[17] Fiedler, col. 4 lines 11-15.
[18] Fiedler, col. 4 lines 11-15.
[19] Office Action, pg. 11.

patentability of the present application, is respectfully requested in the next official communication. Applicant is proceeding under the assumption that the Office Action intended to make the rejection under § 103(a) using Fiedler, Haq and Varma.

Applicant respectfully traverses the rejection. Claim 13 depends on base claim 1. As set forth above, Applicant believes that base claim 1 is allowable at least for the reason that Fiedler does not teach or suggest all of the elements of the base claim. The addition of Haq and Varma fail to provide the missing elements.

Additionally, a showing of a proper motivation to combine Varma with Fiedler is lacking. Varma relates to a transceiver circuit and "an over-voltage sense circuit ... arranged to detect the over-voltage condition on a data line in the transceiver."[20] Fiedler "relates ... to a differential-to-CMOS level converter having a cross-over voltage adjustment."[21] The Office Action states that it would have been obvious to make the combination in "order to protect transceivers from over-voltages.[22] However, Fiedler does not teach or suggest transceivers and the suggested motivation to combine only restates an advantage of Varma. Therefore, one of ordinary skill in the art would not be lead to combine the transceiver circuit of Varma with the differential-to-CMOS level converter of Varma.

Further, a showing of a proper motivation to combine Haq and Fiedler is lacking. Fiedler relates to a differential-to-CMOS level converter.[23] Haq refers to a master [device] 205 configured to communicate twenty signals including single ended-signals S0-S17 and small-swing complementary-source synchronous voltage and timing references SSVTR and /SSVTR.[24] Haq also refers to where a slave [device] 210 may include multiple receivers (405 in FIG. 4) wherein each receiver 405 includes two comparators, one for comparing the signal against SSVTR and the other for comparing the signal against /SSVTR.[25] Thus, Haq does not disclose receiving SSVTR and /SSVTR differentially, but receives single ended signals with SSVTR or /SSVTR. Therefore, Haq does not describe a cross-over voltage on a differential communication bus. Haq also refers to

[20] Varma, Abstract.
[21] Fiedler, col. 1 lines 13-16.
[22] Office Action, pg. 11.
[23] Fiedler, Abstract.
[24] Haq, col. 6 lines 31-35.
[25] Haq, col. 6 lines 45-49.

high frequency signaling requiring small signal amplitudes to consume reasonable power,[26] such as 0.5v.[27] Thus, one of ordinary skill in the art would not be lead to combine Haq with a device using the CMOS levels in Fiedler to drive signals on a communication bus.

Furthermore, Haq refers to where the system and method advantageously eliminate the need for a high-impedance VREF signal for comparison of small-swing single-ended signals.[28] Haq also explicitly states that there is no VREF (reference voltage) for comparison with the signal voltage,[29] and lists advantages of doing so.[30] Fiedler relies on comparing the cross-over voltage to a reference voltage.[31] Thus, Haq teaches away from the voltage reference comparison of Fiedler and one of ordinary skill in the art would not be led to combine Haq with Fiedler.

Applicant respectfully requests reconsideration and allowance of claim 13.

3. Claims 25-31 were rejected under 35 USC § 103(a) as being unpatentable over Haq (U.S. 6,430,606) in view of Fiedler (U.S. 5,726,588). Applicant respectfully traverses the rejection.

The proposed combination of Haq and Fiedler fails to teach or suggest all of the elements of the claims. Applicant cannot find in Haq with Fiedler any teaching or suggestion of, among other things,

> wherein the cross-over lock feedback circuit generates a correcting voltage as a function of a mismatch in switching times between the positive conductor and the negative conductor,

as presently recited in the claims. Instead, Fiedler compares the cross-over voltage to a reference voltage, and sources or sinks equal offset currents into or from circuit nodes N6 and $\overline{N6}$ in response to the comparison.[32]

Additionally, the Office Action fails to establish a *prima facie* case of obviousness because, as set forth previously, a showing of a proper motivation to combine Haq with Fiedler is lacking. Applicant respectfully requests reconsideration and allowance of claims 25-31.

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[26] Haq, col. 1 lines 45-46.
[27] Haq, col. 9 lines 15-18.
[28] Haq, col. 3, lines 40-47
[29] Haq, col. 12, lines 45-50.
[30] Haq, col. 1 lines 53-55, col. 3 lines 42-47, and col. 12 lines 45-50.
[31] Fiedler, col. 4 lines 11-15.
[32] Fiedler, col. 4 lines 11-15.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at 612-371-2172 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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